RS-Enhanced TCM for Multilevel Flash Memories

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***Abstract*—Multilevel flash memories store more than one bit per storage cell and are further characterized by large word (page) sizes and very low target error rates. In this paper, a high-rate error control scheme is presented that uses inner trellis-coded modulation (TCM) for storing two bits per cell with five possible charge levels. The coded subset-label bits and the uncoded signal-label bits of TCM are independently protected by separate outer Reed-Solomon (RS) codes. The resulting scheme permits multistage decoding. Errors made by the TCM decoder in the subset-label bits occur in bursts and are corrected by the associated first RS decoder prior to determining signal-label bits and correcting errors in those bits by the associated second RS decoder. The multi-stage decoding avoids the significant spread of errors from subset-label bits into the generally larger number of signal-label bits which is typical for conventional serial RS-TCM concatenation when the inner TCM system operates at relatively low SNR. The error performance of the proposed scheme is evaluated at low error rates by a mixed simulation-analytic method. It is shown that the proposed scheme exhibits highly favorable performance vs. complexity tradeoffs compared to the other schemes.**

***Index Terms*—Trellis-coded modulation, Reed-Solomon codes, multi-level coded-modulation, flash memory.**

I. Introduction

TRELLIS-CODED modulation (TCM) is a well-established error-correction method [1], [2] that has been extensively studied [3]–[8] and employed in a wide range of applications such as satellite communications [9], telephone-line modems [10], high-speed digital subscriber loops [11], cable modems, etc. TCM can be viewed as a special case of multi-level coded-modulation (MLCM). In general, MLCM is based on partitioning a higher order constellation of modulation symbols successively into subsets with increasing intra-subset distances and applying appropriate coding at different levels of the set-partitioning tree [12]. To achieve reliable communication without bandwidth expansion compared to uncoded schemes operating at the same spectral efficiency, TCM typically uses redundant 1 - 4 dimensional symbol constellations with convolutional coding of the subset-label bits associated with the lower set-partitioning levels and leaving the remaining signal-label bits uncoded. TCM decoding can be considered as deciding first on the most likely sequence of subset-labels and then determining the signal-labels of the most likely symbol in each subset. The concatenation of TCM with outer Reed-Solomon (RS) coding has been widely studied in [13]–[15] and applied in standard physical-layer technologies [16]. Usually, all bits entering the TCM encoder are equally protected by a single outer layer RS code and symbol interleaving. The only exception appears to be the scheme of [15] where the outer RS coding is applied only to the signal-label bits of TCM in an effort to improve immunity to both Gaussian and impulse noise.

For multi-level NAND flash memories, serial RS-TCM concatenation is considered in [17] and serial concatenation of outer Bose-Chaudhuri-Hocquemghem (BCH) coding with inner multi-dimensional TCM is investigated in [18]. With non-binary charge levels more than one information bit per memory cell can be stored, e.g., $4 = 2^2$ distinctive levels for storage of 2 bits per memory cell. Information is written into and retrieved from such memories in words (pages) of typically 4K bytes or longer. Target values for word error rates (WERs) are extremely low, e.g., 10^{-16} [18]. With strong outer RS or BCH coding and inner TCM of modest complexity [13]–[15], [17], [18], the inner TCM decoder can operate at a signal-to-noise ratio (SNR) where bursts of errors in the decoded subset-labels occur relatively frequently compared to the desired target WER. Each erroneously decoded subset label causes with high probability additional errors in the generally larger number of signal-label bits. Such spreading of errors increases the error-correction capability required for a single layer of outer coding. Thus, in conventional RS-TCM concatenation, higher code redundancy leading to lower storage density and/or increased decoding complexity and/or latency are needed.

In this paper, we consider a concatenation of TCM with outer RS coding for the specific application in multi-level NAND flash memories. In contrast to conventional RS-TCM concatenation, however, TCM subset labels and TCM signal labels are protected by separate outer RS coding. The proposed sturcture retains the property of an MLCM scheme. The first level of encoding is comprised of an RS encoder followed by a convolutional encoder to produce subset labels. The second level of encoding generates RS-encoded signal labels. Information bits are recovered from noisy signals by multi-stage decoding. In the first decoding stage subset labels are obtained by Viterbi decoding, followed by first-level RS error correction and re-encoded to specify subset labels. At the target SNR, the recovered subset labels can now be assumed to be correct with high probability. Then in the second decoding stage signal labels are decoded and second-level

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RS corrections are made. The multistage decoding essentially prevents the spread of subset-label bit errors into signal-label bits. Therefore, the proposed scheme requires less RS-coding redundancy than needed in a system with conventional RS-TCM concatenation to achieve comparable error performance. Moreover, the allocation of a given overall coding redundancy to the two outer RS encoders can be optimized by considering the different requirements for protecting subset labels and signal labels.

The proposed error-control system also offers several advantages in computational decoding complexity. One advantage results, of course, from the reduced error-correction capability needed for outer RS coding. Other advantages stems from the fact that RS decoding of subset-label bits and signal-label bits can individually be stopped after the syndrome calculation step when zero syndromes are obtained.

At the extremely low target WERs of flash memories, error performance cannot be determined by Monte-Carlo simulations. The performance of the proposed system is evaluated by a mixture of simulation and analysis to obtain an estimated tight upper bound on the WER. This method is used to determine for a given operating SNR and inner TCM scheme the parameters of the outer RS encoders needed to achieve a given target WER.

The rest of the paper is organized as follows. Section II provides a detailed description of the proposed error control solution for a given inner TCM scheme and discusses design parameters. The method for estimating WER is presented in Section III. In Section IV performance results are given for the proposed system, and performances are compared with those of stand-alone BCH, RS, and LDPC coding as well as traditional RS-TCM code concatenation. Section V presents conclusions.

II. The Proposed Scheme

Each NAND flash memory cell is comprised of a metal-oxide-semiconductor field-effect transistor (MOSFET) transistor with a floating gate. The amount of charge stored during writing in the floating gate is quantized to q values and thus a cell can store $\log_2 q$ bits of information. During reading the charge on the floating gate is measured by sensing the threshold voltage of the transistor. To improve flash memory storage density, aggressive technology scaling has been persistently pursued together with error control coding to cope with effects of noise, interference between cells, and variations of cell properties. In essence, the flash memory can be modeled as a noisy communication channel, and the errors can be efficiently corrected by utilizing error-correcting codes which have been critical in the deployment of virtually all modern communication systems.

The proposed error-control scheme is shown in Figs. 1 and 2. In Fig. 1, a data word m is first divided into two blocks b_s and b_u. The block b_u is further divided into L sub-blocks, each of which is fed into one of L identical RS encoders, $\mathrm{EC_u}$. The block b_s is encoded by the RS encoder, $\mathrm{EC_s}$. The RS encoders $\mathrm{EC_s}$ and $\mathrm{EC_u}$ provide RS codewords $\mathcal{C}_s$ and $\{\mathcal{C}_u^{(0)}, \ldots, \mathcal{C}_u^{(L-1)}\}$, respectively. The TCM encoder consists of a convolutional encoder and a signal mapper. The codeword $\mathcal{C}_s$ is segmented into inputs to the convolutional encoder which produces subset labels $\mathcal{C}_{cs}$. The codewords $C_u^{(j)}$ for $0 \le j \le L-1$ are segmented into signal labels $\mathcal{C}_u$. The signal mapper translates each subset label into a subset of a multi-dimensional signal set and uses a signal label to select a particular multi-dimensional signal in this subset. The output word from the mapper is denoted by $\mathcal{C}$. The one dimensional component signals of $\mathcal{C}$ are then stored as charges in flash memory cells.

The decoder depicted in Fig. 2 receives a sequence r of sensed threshold voltages representing stored charges which have been corrupted after the floating-gates were programmed. The multi-dimensional demodulator $\mathrm{MD_1}$ converts the sequence into the input sequence r_{cs} to the Viterbi decoder. The obtained output sequence r_s is decoded by the decoder $\mathrm{DC_s}$ into an estimate of the block b_s which is denoted by $\hat{b}_s$ in Fig. 2. From $\hat{b}_s$, a sequence of subset labels $\hat{\mathcal{C}}_{cs}$ is obtained by RS re-encoding $\mathrm{EC_s}$ and convolutional re-encoding $\mathrm{EC_{cs}}$. From the received sequence r and the subset label sequence $\hat{\mathcal{C}}_{cs}$, the multi-dimensional demodulator $\mathrm{MD_2}$ estimates sequences of signal labels $r_u^{(j)}$ for $0 \le j \le L-1$. These sequences are decoded by the decoders $\mathrm{DC_u}$ into estimates of blocks $b_u^{(j)}$ for $0 \le j \le L-1$. The estimates of blocks ($\hat{b}_s$ and $\{\hat{b}_u^{(0)}, \ldots, \hat{b}_u^{(L-1)}\}$) form the overall decoder output $\hat{m}$. Reading of m fails if at least one of the RS decoders fails to determine an RS codeword.

For the performance evaluation of the proposed scheme presented in Sections III and IV, we consider an error-control system for 2 bits per cell flash memories, i.e. four charge levels in a cell. In the designed system, 4-dimensional (4-D) TCM [5], [18] is employed as inner coding. The 4-D signal constellation introduced in [5] is a finite subset of the 4-D cubic lattice $\mathbb{Z}^4$ which is simply a direct product of the square lattice $\mathbb{Z}^2$. For the set partitioning step in TCM coding, $\mathbb{Z}^4$ is partitioned into $2^3 = 8$ subsets, $\mathbb{Z}_i^4$ for $i = 0, \ldots, 7$. First, the 2-dimensional (2-D) integer lattice $\mathbb{Z}^2$ has the binary set-partitioning chain $\mathbb{Z}^2(1)/R\mathbb{Z}^2(2)/2\mathbb{Z}^2(4)$, where the values in the parentheses are the minimum squared Euclidean subset distances (MSESD). Hence, $\mathbb{Z}^2$ can be partitioned into 4 sublattices $\mathbb{Z}_i^2$ for $i = 0, \ldots, 3$, which are scaled and translated versions of $\mathbb{Z}^2$ with MSESD=4. Specifically, let $\mathbb{Z}_0^2 = 2\mathbb{Z}^2$, $\mathbb{Z}_2^2 = 2\mathbb{Z}^2 + (1,1)$, $\mathbb{Z}_1^2 = 2\mathbb{Z}^2 + (1,0)$ and $\mathbb{Z}_3^2 = 2\mathbb{Z}^2 + (0,1)$. Now, the subsets, $\mathbb{Z}_i^4$'s are constructed by taking unions of two direct products, $\mathbb{Z}_i^2 \times \mathbb{Z}_j^2$ for $0 \le i, j \le 3$. That is, $\mathbb{Z}_i^4 = (\mathbb{Z}_{i_1}^2 \times \mathbb{Z}_{i_2}^2 \cup \mathbb{Z}_{i_3}^2 \times \mathbb{Z}_{i_4}^2)$ such that $\bigcup_{i=1}^{8} \mathbb{Z}_i^4 = \mathbb{Z}^4$, and $\bigcap_{i=1}^{8} \mathbb{Z}_i^4 = \emptyset$. Specifically, one possible choice is

$$\mathbb{Z}_0^4 = (\mathbb{Z}_0^2 \times \mathbb{Z}_0^2 \cup \mathbb{Z}_2^2 \times \mathbb{Z}_2^2),\ \mathbb{Z}_1^4 = (\mathbb{Z}_0^2 \times \mathbb{Z}_1^2 \cup \mathbb{Z}_2^2 \times \mathbb{Z}_3^2),$$
$$\mathbb{Z}_4^4 = (\mathbb{Z}_0^2 \times \mathbb{Z}_2^2 \cup \mathbb{Z}_2^2 \times \mathbb{Z}_0^2),\ \mathbb{Z}_5^4 = (\mathbb{Z}_0^2 \times \mathbb{Z}_3^2 \cup \mathbb{Z}_2^2 \times \mathbb{Z}_1^2),$$
$$\mathbb{Z}_2^4 = (\mathbb{Z}_1^2 \times \mathbb{Z}_1^2 \cup \mathbb{Z}_3^2 \times \mathbb{Z}_3^2),\ \mathbb{Z}_3^4 = (\mathbb{Z}_1^2 \times \mathbb{Z}_2^2 \cup \mathbb{Z}_3^2 \times \mathbb{Z}_0^2),$$
$$\mathbb{Z}_6^4 = (\mathbb{Z}_1^2 \times \mathbb{Z}_3^2 \cup \mathbb{Z}_3^2 \times \mathbb{Z}_1^2),\ \mathbb{Z}_7^4 = (\mathbb{Z}_1^2 \times \mathbb{Z}_0^2 \cup \mathbb{Z}_3^2 \times \mathbb{Z}_2^2).$$

Hence, $\mathbb{Z}^4$ can be partitioned into 8 subsets $\mathbb{Z}_i^4$ for $i = 0, \ldots, 7$, which are scaled, translated and rotated versions of the densest 4-D lattice D_4 [19] with MSESD=4. The minimum Euclidean distance between two signal points in $\mathbb{Z}_i^4$ will be

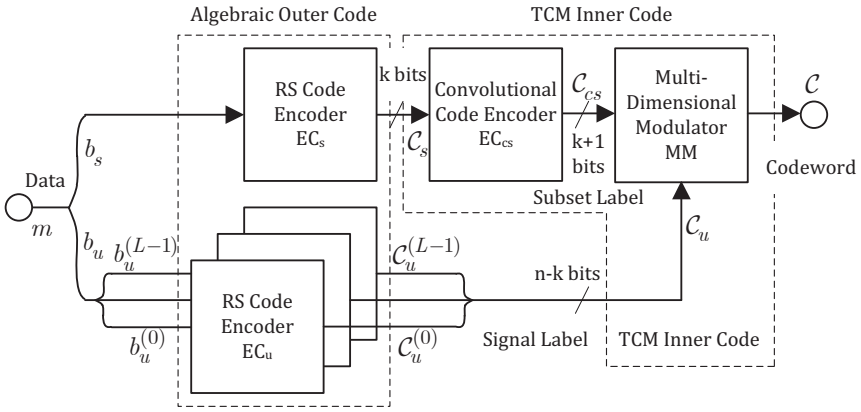

Fig. 1. Block diagram of the encoder of the proposed error-control system.

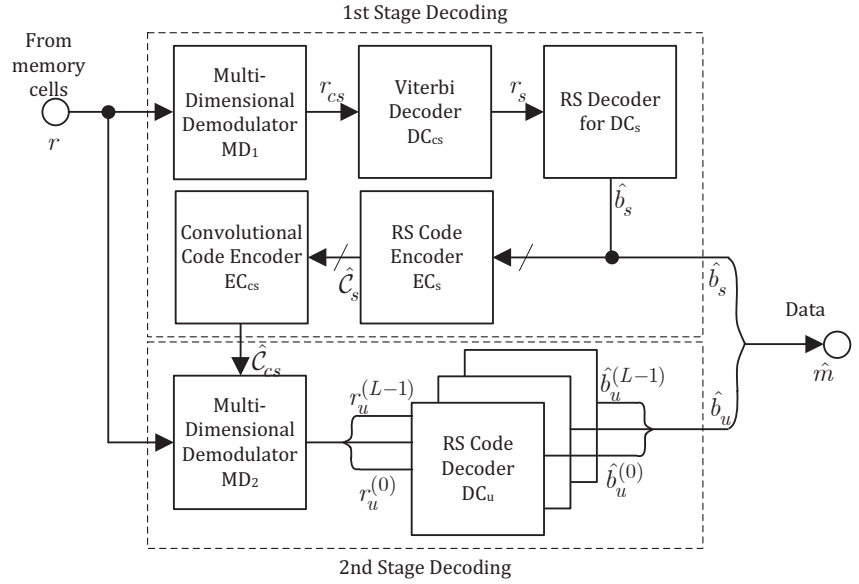

Fig. 2. Block diagram of the decoder of the proposed error-control system.

denoted by $d_{RD_4} = 2d_0$ [1] where d_0 is the minimum Euclidean distance between two signal points in $\mathbb{Z}^2$.

The 4-D signal constellation, a subset of $\mathbb{Z}^4$, is defined by two square shaping regions S_1 and S_2 in such a way that $\mathbb{Z}^4(S = S_1 \times S_2) = \mathbb{Z}^2(S_1) \times \mathbb{Z}^2(S_2)$ where $\mathbb{Z}^2(S_i) = \mathbb{Z}^2 \cap S_i$ for $i = 1, 2$. Thus, there are an equal number of points in each dimension of S_i. We assume that each TCM symbol in $\mathbb{Z}^4(S)$ represents 9 coded bits. Then, the number of points in each dimension, ℓ, must satisfy the inequality $2^9 \leq \ell^4$, and the minimum value of ℓ becomes 5. We consider the particular choices: $S_1 = \{(s_1, s_2) | 0 \leq s_1 \leq 4, -1 \leq s_2 \leq 3\}$ and $S_2 = \{(s_1, s_2) | -1 \leq s_1 \leq 3, 0 \leq s_2 \leq 4\}$[2] since they make the number of points in each subset $\mathbb{Z}_i^4(S)$ almost uniform where

$$\mathbb{Z}_i^4(S) = (\mathbb{Z}_{i_1}^2(S_1) \times \mathbb{Z}_{i_2}^2(S_2) \cup \mathbb{Z}_{i_3}^2(S_1) \times \mathbb{Z}_{i_4}^2(S_2)),$$
$$\mathbb{Z}_i^2(S_j) = \mathbb{Z}_i^2 \cap S_j.$$

[1]In [20], partitioning $\mathbb{Z}^4$ into 8 subset is governed by the set partitioning chain $\mathbb{Z}^4/D_4/R\mathbb{Z}^4/RD_4$, and it can be shown that the minimum Euclidean distances of $\mathbb{Z}_i^4$ and RD_4 are the same.

[2]We assume that a memory cell has five different charge levels each of which represents a signal value of s_i.

The signal point in each dimension is stored in a flash memory cell in which there must be five possible charge levels. Since we consider 2 bits per cell flash memories, the number of charge levels is expanded by one. Accordingly, the data stored in flash memory cells can be understood as 5-level pulse amplitude modulation (5-PAM) symbols. A 4-D TCM with 5-PAM signals to transmit 2 bit/dimension is also employed in [21] using an 8-state convolutional encoder.

For the TCM coding shown in Fig. 1, the encoder $\mathrm{EC_{cs}}$ for a rate 2/3 convolutional code has a parity-check matrix [2]

$$H(D) = [D^3 + D^2, D, D^4 + 1]$$

which takes 2 message bits and produce a 3 bit subset label which specifies a subset of the 4-D signal constellation $\mathbb{Z}_i^4(S)$ for $0 \leq i \leq 7$. The mapping from a subset label to a subset $\mathbb{Z}_i^4(S)$ is designed such that the 8 subsets are equally used in the outgoing and incoming branches from and to a node in the trellis diagram corresponding to the 16-state convolutional code. A point in $\mathbb{Z}_i^4(S)$ is specified by a 6-bit signal label. Then, a TCM symbol in $\mathbb{Z}^4(S)$ represents a total of 9 coded bits for 8 message bits. However, it should be noted

that there are $5^4 = 625$ possible points in $\mathbb{Z}^4(S)$ whereas the multi-dimensional modulator has as its input 9 bits per TCM symbol which amount to $2^9 = 512$ signal points. Thus, $625 - 512 = 113$ points should be excluded. When TCM is used in communication systems, the 512 points are typically selected so as to minimize the average power. However, the NAND flash memory channel can be viewed as a peak-power-limited channel and minimizing average power does not help. In fact, in practical flash memory channels, the signal points may be selected in such a way that the interference due to combinations of stored charges in physically adjacent cells is minimized [22], [23]. For the analysis in this paper, we arbitrarily choose 512 signal points such that the peak power is not increased. We now have subsets $\tilde{\mathbb{Z}}_i^4$ for $i = 0, 1, \ldots, 7$.

A codeword $\mathcal{C}$ represents user data m of length 4KB, which is a minimum word size in flash memory to be written in a batch. The 4KB data are divided into four 1 KB data streams, and the first data stream corresponding to b_s is encoded by the RS encoder, ECs. The remaining three 1KB streams denoted as $b_u^{(0)}$, $b_u^{(1)}$ and $b_u^{(2)}$ in Fig. 1 are encoded by $\mathrm{EC_u}$ independently. Both RS codes $\mathcal{C}_u$ and $\mathcal{C}_s$ are defined over $\mathrm{GF}(2^{10})$. The rates of $\mathcal{C}_s$ and $\mathcal{C}_u$ depend on the numbers of redundant bits required to achieve the target WER. In the next section, we shall evaluate the performance of the proposed concatenation scheme and show how to select the design parameters such that the error-correcting capabilities of $\mathrm{EC_s}$ and $\mathrm{EC_u}$ achieve a target WER.

III. Performance Evaluation Method

In this section we analyze the decoding failure rate P_{df} for the proposed scheme, which is given by

$$P_{\mathrm{df}} = P_{\mathrm{df_s}} + (1 - P_{\mathrm{df_s}}) \left(1 - \prod_{j=0}^{L-1} (1 - P_{\mathrm{df_u}}^{(j)}) \right) \approxeq P_{\mathrm{df_s}} + \sum_{j=0}^{L-1} P_{\mathrm{df_u}}^{(j)},$$

where $P_{\mathrm{df_s}}$ and $P_{\mathrm{df_u}}^{(j)}$ are the probabilities of decoding failures of the RS decoders $\mathrm{DC_s}$ and $\mathrm{DC_u}$, respectively. In the regime of very small word error rates $\mathrm{WER} \leq \mathrm{WER_{tgt}} = 10^{-16}$, the probabilities that $\mathrm{DC_s}$ and $\mathrm{DC_u}$ produce wrong codewords can be ignored because in the high SNR regime the probabilities of such decoding errors are negligible compared to the probabilities of decoding failure. Thus P_{df} can be regarded as WER.

We define the signal-to-noise ratio of noisy read signals in dB as $\mathrm{SNR_{pp}} = 20 \log_{10}(\mathrm{V}/\sigma)$, where σ is the standard deviation of assumed i.i.d. additive white Gaussian noise (AWGN), and V is the difference between highest and lowest threshold voltages of a cell. For M levels equally spaced by d_0, V is set to $(M-1)d_0$.

The data stream for the subset label bits is first decoded by a Viterbi decoder whose outputs exhibit burst error behavior. The systematically encoded bits therein are then assembled into a received sequence r_s to be decoded by $\mathrm{DC_s}$. From simulation results we capture in a modified Gilbert model the error behavior of the RS symbols caused by burst errors in the decoded subset labels. This enables us to compute analytically the decoding failure probability for a received (N_c, t_c) RS codeword $\mathcal{C}_s$.

If decoding by $\mathrm{DC_s}$ is successful, the re-encoded subset labels can be assumed to be error-free. We analyze the probability of erroneous maximum likelihood (ML) signal decoding within signal subsets selected by correct subset labels. We also investigate the translation of erroneous signal labels into erroneous RS symbols to obtain the probabilities of the number of erroneous RS symbols within blocks of given length. As for $\mathcal{C}_u$, the decoding failure probability can then be computed analytically for received (N_u, t_u) RS codewords $\mathcal{C}_u^{(j)}$.

The evaluations are possible because inner TCM decoding operates at error rates much higher than the low WERs of interest, where $P_{\mathrm{df_s}}$ and $P_{\mathrm{df_u}}^{(j)}$ cannot directly be determined by computer simulation [14].

A. Analysis for Subset Label Bits

In the sequence of subset labels r_s obtained by the Viterbi decoder $\mathrm{DC_{cs}}$, burst errors occur. The length and frequency of the bursts depend on the convolutional code employed for TCM encoding and the operating $\mathrm{SNR_{pp}}$. In the proposed scheme two systematically encoded bits from five consecutively decoded subset labels are mapped into one 10-bit RS symbol. In a received sequence r_s of length N_c symbols, error bursts in the subset labels can cause one RS symbol or two and occasionally more than two consecutive RS symbols to be in error. Interleaving of RS symbols in multiple codewords $\mathcal{C}_s$ is not employed. It could make sense in other designs especially for longer data words than 4K bytes. While bursts errors at the Viterbi decoder output are well represented by a Gilbert model [24], the resulting burst error behavior of the RS symbols is better described by the modified Gilbert model [14] shown in Fig. 3. This model consists of a good state G and two bad states, B_1 and B_2. An erroneous RS symbol occurs whenever one of the bad states is reached. The transition probabilities P_{gg}, P_{gb_1}, P_{b_1g}, $P_{b_1b_2}$, P_{b_2g}, and $P_{b_2b_2}$ are estimated by computer simulation [13], [14].

For analyzing the occurrence of symbol errors in sequences governed by the state transition diagram of Fig. 3, we use the augmented state-transition probability matrix

$$\mathbf{P}_{\mathrm{tr}}(X) = \begin{bmatrix} P_{gg} & P_{gb_1} \cdot X & 0 \\ P_{b_1g} & 0 & P_{b_1b_2} \cdot X \\ P_{b_2g} & 0 & P_{b_2b_2} \cdot X \end{bmatrix}$$

where X is an indeterminate variable introduced for counting errors. For example, $P_{gb_1}X$ characterizes a transition from G to B_1 with probability P_{gb_1} and the occurrence of one error. The properties of sequences of length N_c are obtained by considering $\mathbf{P}_{\mathrm{tr}}(X)^{N_c}$. We assume that sequences start and end in state G. Then the probability of having i_c erroneous symbols in a sequence of length N_c is given by the coefficient of X^{i_c} in the polynomial $\left[\mathbf{P}_{\mathrm{tr}}(X)^{N_c}\right]_{gg}$, i.e., the element in the top-left position of $\mathbf{P}_{\mathrm{tr}}(X)^{N_c}$. We write this compactly as

$$\Pr[i_c; N_c] = \mathrm{coeff}\left(\left[\mathbf{P}_{\mathrm{tr}}(X)^{N_c}\right]_{gg}, i_c \right).$$

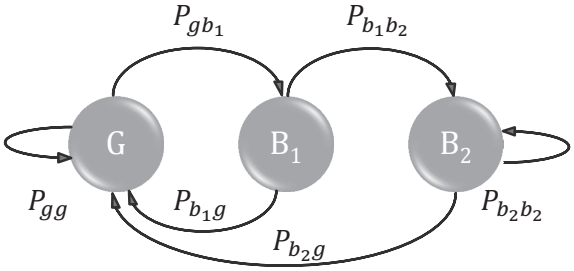

Fig. 3. The state transition diagram of the modified Gilbert model for correlated symbol errors.

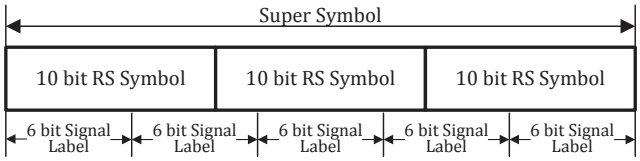

Fig. 4. A super symbol consisting of five signal labels.

The probability of decoding failure for RS (N_c, t_c) codewords C_s becomes

$$P_{\mathrm{df_s}} = \sum_{i_c > t_c} \Pr[i_c; N_c].$$

B. Analysis for Signal Label Bits

In the $\mathrm{SNR_{pp}}$ region of interest, the probability of subset labels errors by ML signal decoding in a correctly determined 4-D signal subset $\tilde{\mathbb{Z}}_i^4$, $i = 0, 1, \ldots, 7$, is well approximated by

$$P_B \approxeq k_a Q\left(\frac{d_{RD_4}}{2\sigma}\right)$$

where $Q(x)$ is the Gaussian tail-integral function, $d_{RD_4} = 2d_0$ is the minimum Euclidean distance between subset signals, and k_a is the average number of nearest neighbor signals. The value $k_a = 9.5274$ is obtained by counting in each of the eight subsets $\tilde{\mathbb{Z}}_i^4$ for each of the 64 subset signals the nearest neighbor signals, i.e., those at distance d_{RD_4}. Let the total count be N_{near}. Then $k_a = N_{near}/512$, where 512 is number of all 4-D signals. In the unbounded sub-lattices $\mathbb{Z}_i^4$, $i = 0, 1, \ldots, 7$, each 4-D signal is uniformly surrounded by $k = 24$ nearest neighbor signals (*kissing number*). For simplified ML signal decoding within the sub-lattices $\mathbb{Z}_i^4$ instead of the finite subsets $\tilde{\mathbb{Z}}_i^4$, k_a should be replaced by $k = 24$.

The further analysis would be straightforward if the number of RS symbol bits m_{rs} would be an integer multiple of the number of signal label bits m_{sl}. However, in the proposed scheme $m_{rs} = 10$ and $m_{sl} = 6$. Hence, when decoded signal labels are mapped into RS symbols one erroneous signal label can affect either only one RS symbol or two adjacent RS symbols. To find statistically independence of error events, super symbols of $\mathrm{lcm}(m_{rs}, m_{sl}) = 30$ bits must be considered. In each super symbol, 3 RS symbols are associated with 5 signal labels as shown in Fig. 4.

Let P_{S_i}, $0 \le i \le 3$, be the probability of i erroneous RS symbols in a super symbol. Define the polynomial $P_S(X) = P_{S_0} + P_{S_1}X + P_{S_2}X^2 + P_{S_3}X^3$. Then the probability of i_u erroneous $(N_u = 3N_{SS}, t_u)$ RS symbols in a codeword $\mathcal{C}_u^{(j)}$ becomes

$$\Pr[i_u; N_{SS}] = \mathrm{coeff}(P_S(X)^{N_{SS}}, i_u),$$

where N_{ss} is the number of super symbols in r_{u}. This permits calculating

$$P_{\mathrm{df_u}}^{(j)} = \sum_{i_u > t_u} \Pr[i_u; N_{SS}].$$

For the probabilities P_{S_i}, $0 \le i \le 3$, we begin with the pessimistic assumption that an erroneous signal label affects all RS symbols in which the signal label occurs entirely or partially. Table I shows all patterns of 0, 1, and 2 erroneous signal labels and the pessimistic numbers of affected RS symbols.

TABLE I
LIST OF ERROR EVENTS CAUSING 0, 1, AND 2 ERRONEOUS SIGNAL LABELS AND THE PESSIMISTIC NUMBERS OF AFFECTED RS SYMBOLS.

Signal label error pattern	i
0 0 0 0 0	0
e 0 0 0 0	1
0 e 0 0 0	2
0 0 e 0 0	1
0 0 0 e 0	2
0 0 0 0 e	1
e e 0 0 0	2
e 0 e 0 0	2
e 0 0 e 0	3
e 0 0 0 e	2
0 e e 0 0	2
0 e 0 e 0	3
0 e 0 0 e	3
0 0 e e 0	2
0 0 e 0 e	2
0 0 0 e e	2
⋮	⋮

Let these tables be extended up to errors in all five signal labels. Addition of the probabilities of signal label error patterns causing the same number of erroneous RS symbols gives

$$P_{S_0} = (1 - P_B)^5 = \bar{P}_B^5$$
$$P_{S_1} \approxeq 3P_B\bar{P}_B^4 \quad (1)$$
$$P_{S_2} \approxeq 2P_B\bar{P}_B^4 + 7P_B^2\bar{P}_B^3 + 2P_B^3\bar{P}_B^2 \approxeq 2P_B\bar{P}_B^4 \quad (2)$$
$$P_{S_3} \approxeq 3P_B^2\bar{P}_B^3 + 8P_B^3\bar{P}_B^2 + 5P_B^4\bar{P}_B + P_B^5 \approxeq 0 \quad (3)$$

Numerical evaluations at $\mathrm{SNR_{pp}} = 24\,\mathrm{dB}$ ($P_B = 3.5 \times 10^{-4}$) with the pessimistic approximations of P_{S_1}, P_{S_2}, P_{S_3} in (1), (2), (3) show negligible effect when the terms $P_B^\ell \bar{P}_B^{5-\ell} (\ell > 1)$ in (2) and (3) are omitted.

However, a comparison of the computed values of $\Pr[i_u; N_{SS}]$ with simulation results shows that the pessimistic approximation is too crude. It ignores the possibility that an erroneous second signal label may introduce bit errors only in the first or second RS symbol, and likewise that an erroneous fourth signal label may introduce bit errors only in the second or third RS symbol. This calls for a refinement of

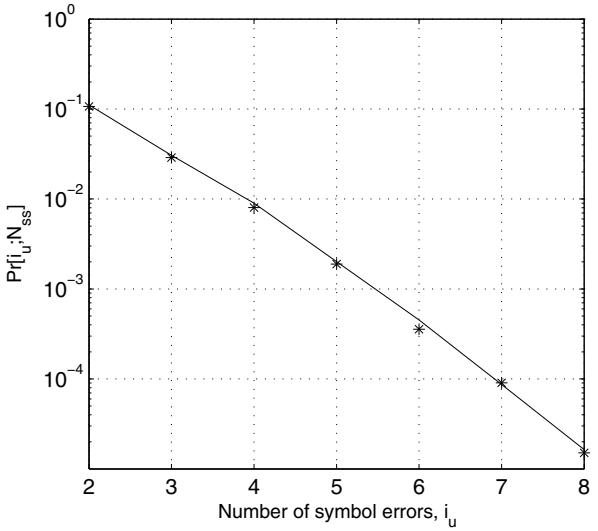

Fig. 5. RS symbol error probabilities at $\mathrm{SNR_{pp}} = 24\,\mathrm{dB}$ and $N_{SS} = 272$; the solid lines represent the upper bounds on the probability of having i erroneous symbols in an RS codeword, and the asterisk symbols show simulation results.

the approximations of P_{S_1} and P_{S_2} as follows:

$$P_{S_1} \cong (3 + \alpha_2 + \alpha_4) P_B \bar{P}_B^4 \tag{4}$$

$$P_{S_2} \cong (2 - \alpha_2 - \alpha_4) P_B \bar{P}_B^4 \tag{5}$$

where α_2 and α_4 are the conditional probabilities

$$\alpha_2 = \Pr\left(\frac{\text{only } 1^{\text{st}} \text{ or } 2^{\text{nd}} \text{ RS symbol wrong}}{\text{error in } 2^{\text{nd}} \text{ signal label}}\right)$$

$$\alpha_4 = \Pr\left(\frac{\text{only } 2^{\text{nd}} \text{ or } 3^{\text{rd}} \text{ RS symbol wrong}}{\text{error in } 4^{\text{th}} \text{ signal label}}\right).$$

For computing α_2 and α_4 we extend the enumeration employed for computing k_a. As for k_a, we count in each of the eight subsets $\tilde{\mathbb{Z}}_i^4$ for each of the 64 subset signals the nearest neighbor signals to obtain the total count N_{near}. In addition we inspect the signal label difference associated with the nearest neighbor signals. The nearest neighbor signals whose signal labels would cause only the 1^{st} or 2^{nd} RS symbol to be wrong are counted as $N_{near.2}$. Similarly, the nearest neighbor signals whose signal labels would cause only the 2^{nd} and 3^{rd} RS symbol to be wrong are counted as $N_{near.4}$. Then $\alpha_2 = N_{near.2}/N_{near}$ and $\alpha_4 = N_{near.4}/N_{near}$.

Figure 5 shows excellent agreement between values of $\Pr[i_u; N_{SS}]$ obtained by computer simulation and computed with the final approximations of P_{S_1} and P_{S_2} as given by (4) and (5).

IV. Performance Results and Comparisons

The proposed error-control system with inner TCM and outer RS coding and those using BCH-only and RS-only coding have been compared utilizing the semi-analytical performance evaluation method. We also consider a conventional RS-TCM concatenation, called simply RS-TCM hereafter in which 16 outer RS codewords are concatenated with inner TCM through an interleaver.

Flash memory devices store charges into the floating gates whose levels are read by measuring threshold voltages. The write-read operations of flash memories can be understood as information transmission-reception over a noisy channel (e.g., an AWGN channel in our work) with M-ary PAM . It should be noted that the inner TCM in the proposed as well as some of existing concatenation schemes is based on expansion of the signal constellation from 4-PAM to 5-PAM, which decreases the distance between adjacent signal points by 25%. This reduction in distance is reflected in the comparative performance evaluation. Note that the competing systems with BCH, RS and LDPC codes use the original 4-PAM signal constellation.

The most popular error-control systems for multi-level flash memory today employ BCH coding only. For such a system, we consider encoding of 4K bytes of data into four BCH codewords $(n, k, t) = (8751, 8192, 40)$, and each of them provides an error-correcting capability t of 40 bits. A target WER of 10^{-16} is achieved at a $\mathrm{SNR_{pp}}$ of 25.2 dB. That is

$$\mathrm{WER} = 1 - (1 - P_{\mathrm{df}})^4 \leq \mathrm{WER_{tgt}} = 10^{-16} \tag{6}$$

where

$$P_{\mathrm{df}} = \sum_{n_e=t+1}^{n} \binom{n}{n_e} P_{\mathrm{raw,x}}^{n_e} (1 - P_{\mathrm{raw}})^{n-n_e},$$

and $P_{\mathrm{raw,x}}^{n_e}$ is replaced with $P_{\mathrm{raw,b}}$ and $P_{\mathrm{raw,s}}$ for raw bit error rate and raw RS symbol error rate, respectively. Therein the BER with the standard Gray mapping of two bits into a 4-PAM signal is given as

$$P_{\mathrm{raw,b}} \cong \frac{3}{4} Q\left(\sqrt{\frac{\mathrm{SNR_{pp}}}{36}}\right).$$

At the same $\mathrm{SNR_{pp}}$, we compute error-correcting capability of an RS code over $\mathrm{GF}(2^{10})$ by choosing the smallest t value with which (6) can be satisfied for an RS symbol error probability of

$$P_{\mathrm{raw,s}} = 1 - \left(1 - \frac{3}{2} Q\left(\sqrt{\frac{\mathrm{SNR_{pp}}}{36}}\right)\right)^5.$$

The evaluation shows that the required error-correcting capability of RS-only coding is achieved with $t = 38$. Thus, a 4K byte data word can be protected by four (896, 820, 38) shortened RS codewords. For code concatenation using conventional method, 16 (255, 239, 8) RS codewords over $\mathrm{GF}(2^8)$ are needed for outer code. The 16 RS codewords are interleaved to randomize the error bursts due to the inner TCM. Since the depth of interleaver is long enough, 16 codewords, the probability of the number of erroneous symbols per codeword can be modeled as a binomial distribution. That is,

$$P_{\mathrm{df}} = \sum_{n_e=t+1}^{n} \binom{n}{n_e} P_s^{n_e} (1 - P_s)^{n-n_e}.$$

where P_s is an average symbol error rate which is calculated from computer simulations on an AWGN channel [13], [14]. Thus, the WER of RS-TCM is calculated as

$$\mathrm{WER} = 1 - (1 - P_{\mathrm{df}})^{16}.$$

Meanwhile, the proposed error-control system needs two

TABLE II
NUMBER OF REDUNDANT BITS TO ACHIEVE A WER OF 10^{-16} AT $\mathrm{SNR_{pp}} = 25.2\,\mathrm{dB}$; SSL AND SGL INDICATE SUBSET LABEL AND SIGNAL LABEL, RESPECTIVELY.

	Proposed	RS-TCM	BCH	RS
SSL	380			
SGL	$220 \times 3 = 660$	128×16	560×4	760×4
Total	1040	2048	2240	3040

types of RS codes over $\mathrm{GF}(2^{10})$, $\mathcal{C}_\mathrm{s}$ and $\mathcal{C}_\mathrm{u}^{(j)}$ for $0 \le j \le 2$. From the design rule introduced in Section III it follows that the two RS codes require values $t_c^* = 19$ and $t_u^* = 11$, respectively, which correspond to a (858, 820, $t_c^* = 19$) RS code for $\mathcal{C}_\mathrm{s}$ and a (842, 820, $t_u^* = 11$) RS code for $\mathcal{C}_u^{(j)}$. To achieve the target WER at a $\mathrm{SNR_{pp}}$ of 25.2 dB, the overall redundancy of the proposed error-control scheme is less than half of the redundancy required for BCH-only coding and RS-TCM and about a third of the redundancy required for RS-only coding. The number of redundant bits of the four systems are summarized in Table II.

Now, we set out to compare the error rate performances of the four error control-systems at the fixed code rate of 0.97, which is the rate of the proposed system in Table II. The parameters of the BCH-only and RS-only coding scheme are set as (8160, 7894, 19) and (816, 790, 13), respectively. Performances of the error-control systems are shown in Fig. 6. It can be seen that at the target WER of 10^{-16}, the proposed system achieves coding gains of 1.2 dB, 2.0 dB and 1.0 dB over the systems using BCH-only coding, RS-only coding and RS-TCM, respectively.

In the evaluation, we find that the inner TCM in the proposed scheme often cleans all the errors, and the decoding for the outer RS codes can be simplified substantially. Note that the syndrome computation step tests whether the decoding for inner TCM has corrected all errors. Accordingly, depending on the result of this test, the RS decoder may not have to pursue the remaining steps - Berlekamp-Massey algorithm, Chien search, and Forney algorithm. This results in significant power consumption reduction for the overall RS decoding process. At $\mathrm{SNR_{pp}}$ = 25.2 dB, the probabilities that the RS decoding for the subset labels and signal labels need the full decoding steps are $1 - P_{gg}^{N_{ss}} = 0.083$ and $1 - (1 - P_B)^{N_B} = 0.0343$, respectively, where N_B is the number of 6 bit blocks in a RS codeword for the signal labels. Thus, only about 8 and 3 percent of RS codewords for the subset labels and signal labels need the full decoding steps, respectively. On the other hand, in the BCH-only and RS-only cases, the probabilities of the event that the full decoding steps must be performed are respectively given by $1 - (1 - P_{\mathrm{raw,b}})^{N_{\mathrm{BCH}}} \ge 0.99$ and $1-(1-P_{\mathrm{raw,s}})^{N_{\mathrm{RS}}} \ge 0.99$ for $N_{\mathrm{BCH}} = 8160$ and $N_{\mathrm{RS}} = 816$. This indicates that virtually all of codewords need the full decoding steps for the BCH and RS-only cases.

In the proposed system we limit the choice of RS codes over the same Galois field, $\mathrm{GF}(2^{10})$ for simplifying the structure. However, if the RS symbol size for $\mathcal{C}_u$ is a multiple of block size, the proposed system becomes more efficient and thus achieves the target WER at a higher code rate. For the proposed system, RS codes over $\mathrm{GF}(2^{10})$ and $\mathrm{GF}(2^{12})$ for $\mathcal{C}_\mathrm{s}$ and $\mathcal{C}_\mathrm{u}$ have been considered, which increases the code rate to 0.98. For the other systems, codes with parameters (8160, 7964, 14), (816, 796, 10), and (255, 249, 3) are considered for BCH-only coding, RS-only coding, and RS-TCM, respectively. The WERs of the four systems versus $\mathrm{SNR_{pp}}$ are compared in Fig. 7 where we find that at the target WER, the proposed system achieves coding gains of 2.0 dB, 2.6 dB and 1.9 dB over the systems using BCH-only coding, RS-only coding and RS-TCM, respectively. The comparison clearly shows the advantages of the proposed system. The performance improvement is mainly due to the fact that the two-stage decoding suppresses error propagation from the subset labels to the signal labels, and such improvement becomes more pronounced as the alphabet size of the TCM symbols grows as compared to conventional RS-TCM concatenation.

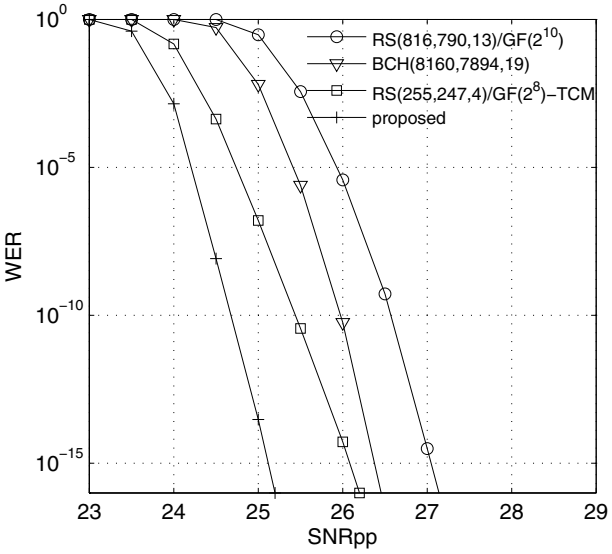

Fig. 6. WERs of the proposed error-control system, RS-only coding, BCH-only coding and conventional RS-TCM at code rates around 0.97.

Figure 8 shows results for the same set of coding schemes with RS codes over $\mathrm{GF}(2^{10})$ at a rate of 0.936. The system with the proposed scheme outperforms BCH-only coding, RS-only coding and RS-TCM, by 0.83 dB, 1.45 dB, and 0.62 dB, respectively, at the target WER. It can be seen that the performance advantage of the proposed scheme is still significant, albeit lower than for the higher coding rate cases. As the code rate gets lower, the relative performance advantage of the proposed concatenation scheme becomes smaller, as expected. This is due to the fact that the convolutional code in the inner TCM starts to loose its error-correcting capability as the operating SNR for the target WER becomes smaller with decreasing code rate, which is the well-known general behavior of error-control systems using TCM coding for high bandwidth efficiency (storage density in our case)[13].

Finally, we consider an error-control system with a low-density parity-check (LDPC) code which also takes advantage of the soft-values from the NAND flash memory. Some of the known LDPC codes have error-floors although they have good threshold behaviors. Here we design a quasi-cyclic LDPC code based on RS code [25] at length of 8820 since it

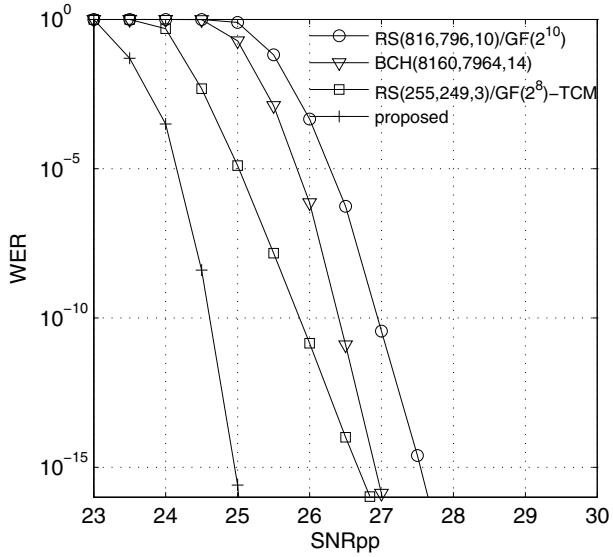

Fig. 7. WERs of the proposed error-control system, BCH-only coding, RS-only coding and RS-TCM at code rates around 0.98.

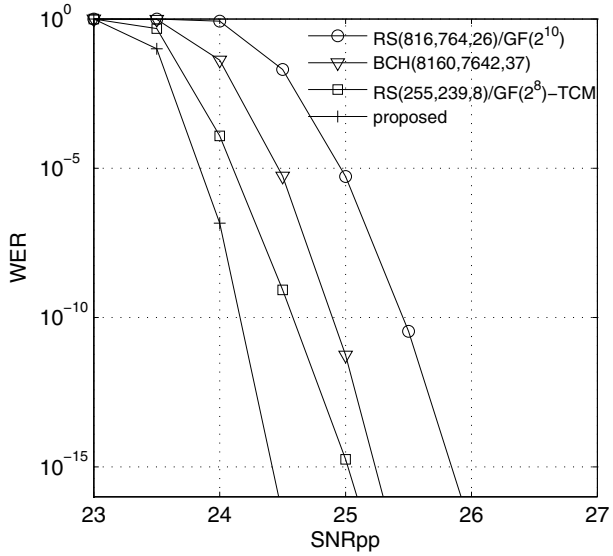

Fig. 8. WERs of the proposed error-control system, BCH-only coding, RS-only coding and RS-TCM at code rates around 0.936.

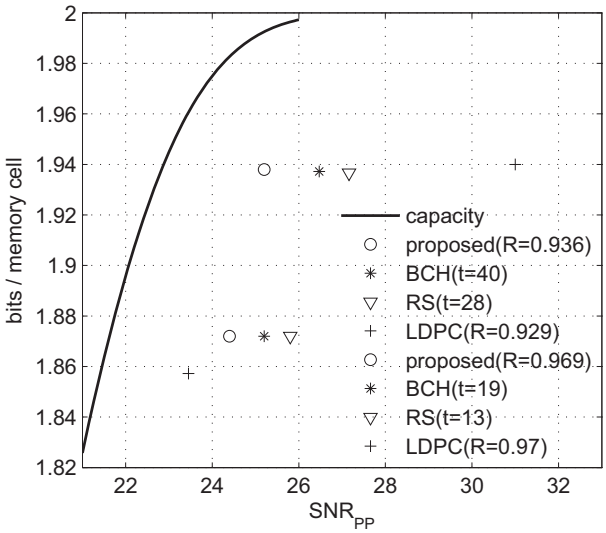

Fig. 9. Required $\mathrm{SNR}_{\mathrm{pp}}$'s to achieve a WER of 10^{-16} with the proposed system, BCH-only coding, RS-only coding, and LDPC codes.

has good error-floor behaviors as well as efficient encoder and decoder structures [26]. The designed LDPC code has a regular structure whose degree distribution pair is given by $\lambda(x) = x^4$ and $\rho(x) = x^{69}$. The sum-product algorithm is used for belief-propagation decoding with a maximum of 50 iterations. The performances of the LDPC code is measured in terms of required $\mathrm{SNR}_{\mathrm{pp}}$ to achieve the target WER and compared with those of the other systems in Fig. 9 where the channel capacity of 4-PAM signal is also shown as a reference. It should be noted that there is no well-established analytical way to evaluate performances of practical LDPC codes at finite lengths, and performances are usually evaluated with Monte-Carlo simulation. However, the target WER of our interest is too low to be estimated with Monte-Carlo simulation; we resort to a linear extrapolation (in log-log scale) of the measured WERs available down to 10^{-8}. The extrapolation gives somewhat optimistic results since the LDPC code is assumed to have no error floors down to the WER of 10^{-16}. Error floors can be estimated to a certain extent using trapping set analysis [27], [28], but even in the optimistic scenario for the LDPC code where the error floors are absent, the proposed scheme yields comparable performance to relative the LDPC codes.

The results indicate that at the code rate 0.93 the LDPC code and the proposed system have respective gaps of 2.21 dB and 2.70 dB from capacity. Thus, the performance of the proposed system is worse than that of LDPC code by only 0.49 dB, which shows that the proposed system has a competitive performance at much reduced complexity. We repeated the evaluations at the code rate of about 0.97. The proposed system is designed at a rate of 0.969, and a (8509, 8256) RS-QC LDPC code is designed with a degree distribution pair, $\lambda(x) = x^2$ and $\rho(x) = x^{67}$ at rate 0.9701. The evaluation results in Fig. 9 show that the proposed system has a capacity gap of 2.4 dB but the LDPC code has a very wide gap of 7.36 dB, even worse than BCH and RS codes based on hard-decision inputs. Our experience with LDPC code designs at high code rates indicates that it is very hard to implement good LDPC codes at high rates for a very low WER, as have been observed elsewhere [29], [30].

V. Conclusions

We proposed an error-control system based on a novel concatenation of RS codes and TCM with application to multi-level NAND flash memories in mind. Burst errors in the subset label bits at the TCM decoder output typically lead to more errors in the generally larger number of signal-label bits when no attempt is made to correct subset-label bit errors prior to determining signal-label bits. Protecting subset-label bits and signal-label bits by separate RS encoding, as done in the proposed concatenation, prevents the spread of subset-label bit

errors into the signal-label bits. It also allows for optimizing the allocation of overall RS coding redundancy by accounting for the different requirements for the two types of bits. We confirm our claims by evaluating and comparing performances of the proposed error-control system and other conventional approaches such as BCH-only coding, RS-only coding, and conventional RS-TCM concatenation with an interleaver using analytical approximations. The comparisons show that the proposed system achieves significant coding gains over the conventional approaches at code rates well above 0.9. A comparison was also made with LDPC coding, and our scheme shows favorable complexity/performance tradeoff in the high rate regime (0.97).

REFERENCES

[1] G. Ungerboeck, "Channel coding with multilevel/phase signals," *IEEE Trans. Inf. Theory*, vol. 28, no. 1, pp. 55–67, Jan. 1982.

[2] ——, "Trellis-coded modulation with redundant signal sets—part I: introduction, and part II: state of the art," *IEEE Commun. Mag.*, vol. 25, no. 2, pp. 5–21, Feb. 1987.

[3] A. Calderbank and J. Mazo, "A new description of trellis codes," *IEEE Trans. Inf. Theory*, vol. 30, no. 6, pp. 784–791, Nov. 1984.

[4] A. Calderbank and N. Sloane, "New trellis codes based on lattices and cosets," *IEEE Trans. Inf. Theory*, vol. 33, no. 2, pp. 177–195, Mar. 1987.

[5] J. Forney, "Coset codes—part I: introduction and geometrical classification," *IEEE Trans. Inf. Theory*, vol. 34, no. 5, pp. 1123–1151, Sep. 1988.

[6] ——, "Coset codes—part II: binary lattices and related codes," *IEEE Trans. Inf. Theory*, vol. 34, no. 5, pp. 1152–1187, Sep. 1988.

[7] J. Forney, G., R. Gallager, G. Lang, F. Longstaff, and S. Qureshi, "Efficient modulation for band-limited channels," *IEEE J. Sel. Areas Commun.*, vol. 2, no. 5, pp. 632–647, Sep. 1984.

[8] L.-F. Wei, "Trellis-coded modulation with multidimensional constellations," *IEEE Trans. Inf. Theory*, vol. 33, no. 4, pp. 483–501, July 1987.

[9] E. Biglieri, "High-level modulation and coding for nonlinear satellite channels," *IEEE Trans. Commun.*, vol. 32, no. 5, pp. 616–626, May 1984.

[10] K. R. McConnell, D. Bodson, and R. Schaphorst, *FAX: Digital Facsimile Technology and Applications*. Artech House, 1992.

[11] B. Saltzberg, T. Hsing, J. Cioffi, and D. Lin, "Special issue on high-speed digital subscriber lines," *IEEE J. Sel. Areas Commun.*, vol. 9, Aug. 1991.

[12] H. Imai and S. Hirakawa, "A new multilevel coding method using error-correcting codes," *IEEE Trans. Inf. Theory*, vol. 23, no. 3, pp. 371–377, May 1977.

[13] R. H. Deng and J. Costello, "High rate concatenated coding systems using multidimensional bandwidth-efficient trellis inner codes," *IEEE Trans. Commun.*, vol. 37, no. 10, pp. 1091–1096, Oct. 1989.

[14] C. Valadon, R. Tafazolli, and B. Evans, "Performance evaluation of concatenated codes with inner trellis codes and outer Reed-Solomon code," *IEEE Trans. Commun.*, vol. 49, no. 4, pp. 565–570, Apr. 2001.

[15] L.-F. Wei, "Two-level coding based on trellis-coded modulation and Reed-Solomon codes," *IEEE Trans. Commun.*, vol. 42, no. 12, pp. 3098–3108, Dec. 1994.

[16] ITU-T Recommendation G.992.3, "Asymmetric digital subscriber line transceivers 2 (ADSL2)," 2005.

[17] A. Ramamoorthy, A. Wu, and P. Sutardja, "Method and system for error correction in flash memory," US Patent 7844879B2, Nov. 2010.

[18] S. Li and T. Zhang, "Improving multi-level NAND flash memory storage reliability using concatenated BCH-TCM coding," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 18, no. 10, pp. 1412–1420, Oct. 2010.

[19] J. Conway and N. Sloane, *Sphere Packings, Lattices and Groups*. Springer-Verlag, 1988.

[20] J. Forney, "Multidimensional constellations—part II: Voronoi constellations," *IEEE J. Sel. Areas Commun.*, vol. 7, no. 6, pp. 941–958, Aug. 1989.

[21] IEEE Standard for Information Technology–Telecommunications and Information Exchange between Systems–Local and Metropolitan Area Networks–Specific Requirements Part 3: Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications - Section Three," IEEE Std. 802.3-2008 (Revision of IEEE Std. 802.3-2005), pp. 1–315, 2008.

[22] G. Dong, N. Xie, and T. Zhang, "On the use of soft-decision error-correction codes in NAND flash memory," *IEEE Trans. Circuits Syst. I: Reg. Papers*, vol. 58, no. 2, pp. 429–439, Feb. 2011.

[23] G. Dong, S. Li, and T. Zhang, "Using data postcompensation and predistortion to tolerate cell-to-cell interference in MLC NAND flash memory," *IEEE Trans. Circuits Syst. I: Reg. Papers*, vol. 57, no. 10, pp. 2718–2728, 2010.

[24] E. N. Gilbert, "Capacity of a burst-noise channel," *Bell Syst. Tech. J.*, vol. 39, pp. 1253–1266, 1960.

[25] L. Chen, I. Djurdjevic, and J. Xu, "Construction of quasicyclic LDPC codes based on the minimum weight codewords of Reed-Solomon codes," in *Proc. 2004 IEEE Int. Symp. Inf. Theory*, p. 239.

[26] Z. Li, L. Chen, L. Zeng, S. Lin, and W. Fong, "Efficient encoding of quasi-cyclic low-density parity-check codes," *IEEE Trans. Commun.*, vol. 54, no. 1, pp. 71–81, 2006.

[27] T. J. Richardson, "Error floors of LDPC codes," in *Proc. 2003 Allerton Conf. Commun., Control Comput.*, pp. 1426–1435.

[28] A. Ramamoorthy and N. Varnica, "Error floors of LDPC coded BICM," in *Proc. 2007 IEEE Int. Conf. Commun.*, pp. 839–844.

[29] F. Chang, K. Onohara, and T. Mizuochi, "Forward error correction for 100 g transport networks," *IEEE Commun. Mag.*, vol. 48, no. 3, pp. S48–S55, 2010.

[30] T. Mizuochi, "Recent progress in forward error correction and its interplay with transmission impairments," *IEEE J. Sel. Topics Quantum Electron.*, vol. 12, no. 4, pp. 544–554, 2006.

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